

FIG. 1

(PRIOR ART)

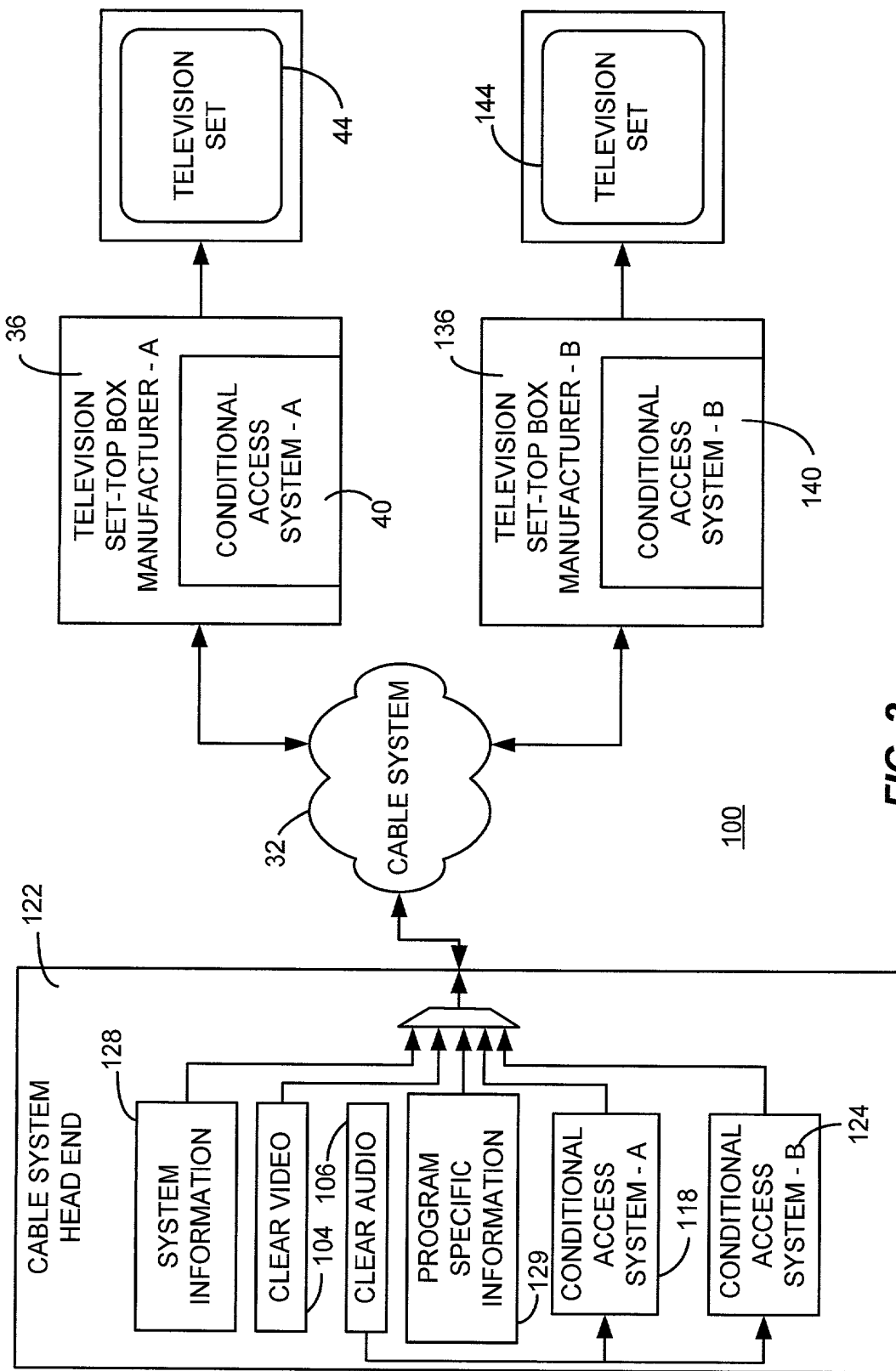


FIG. 2

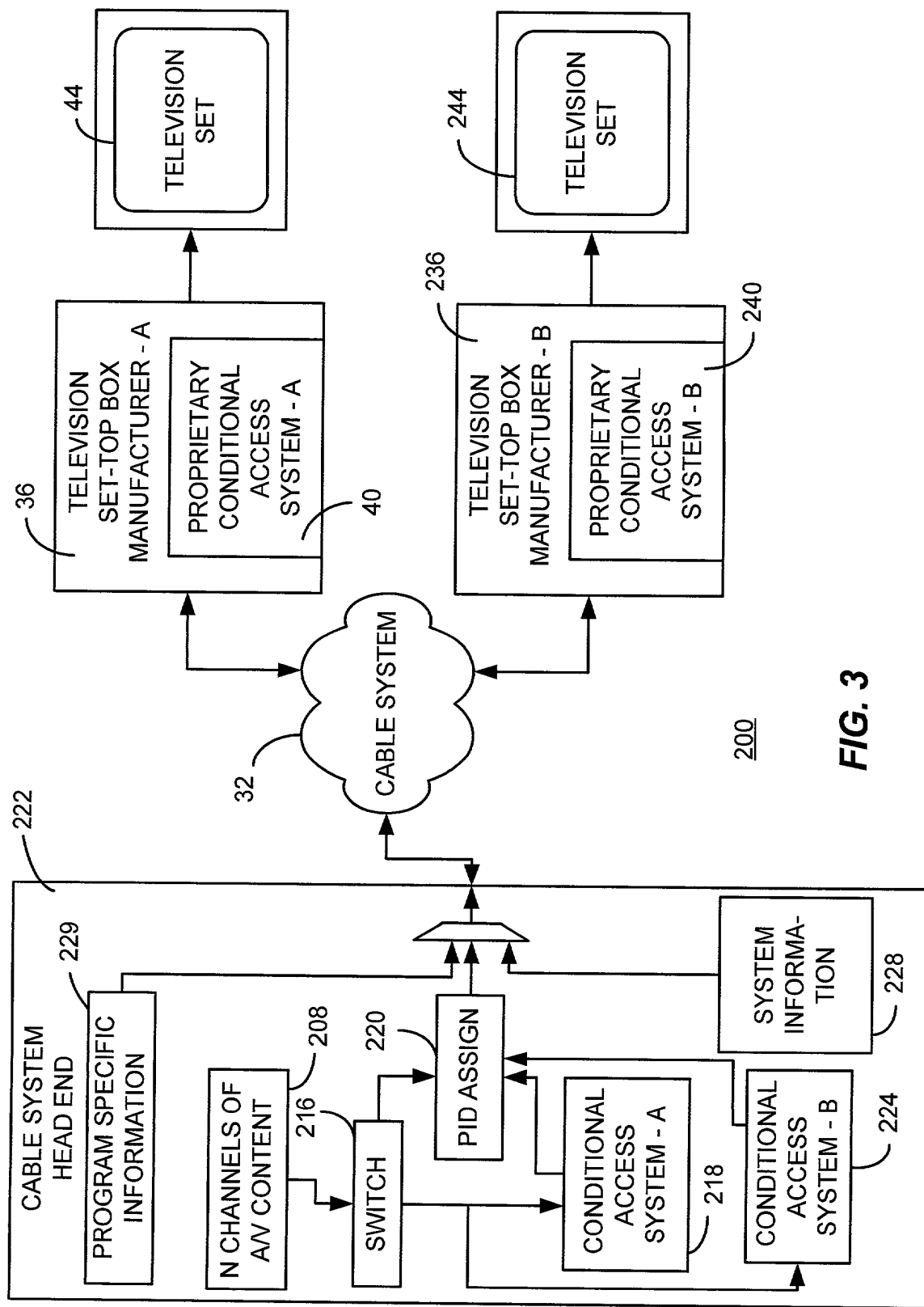


FIG. 3

FIG. 4

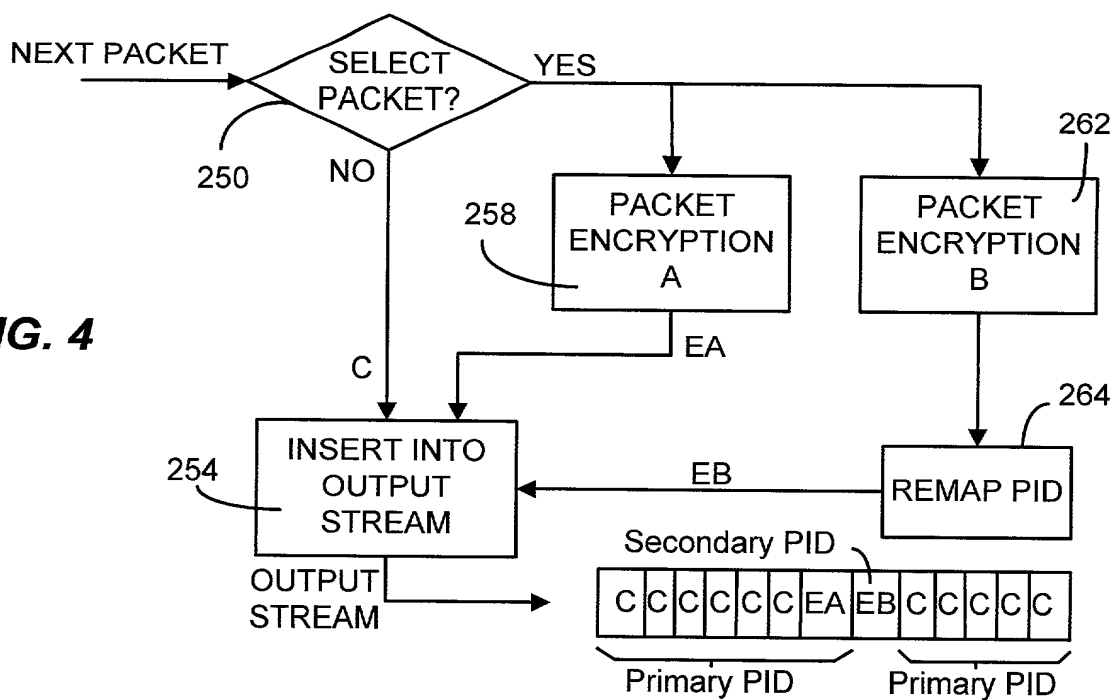
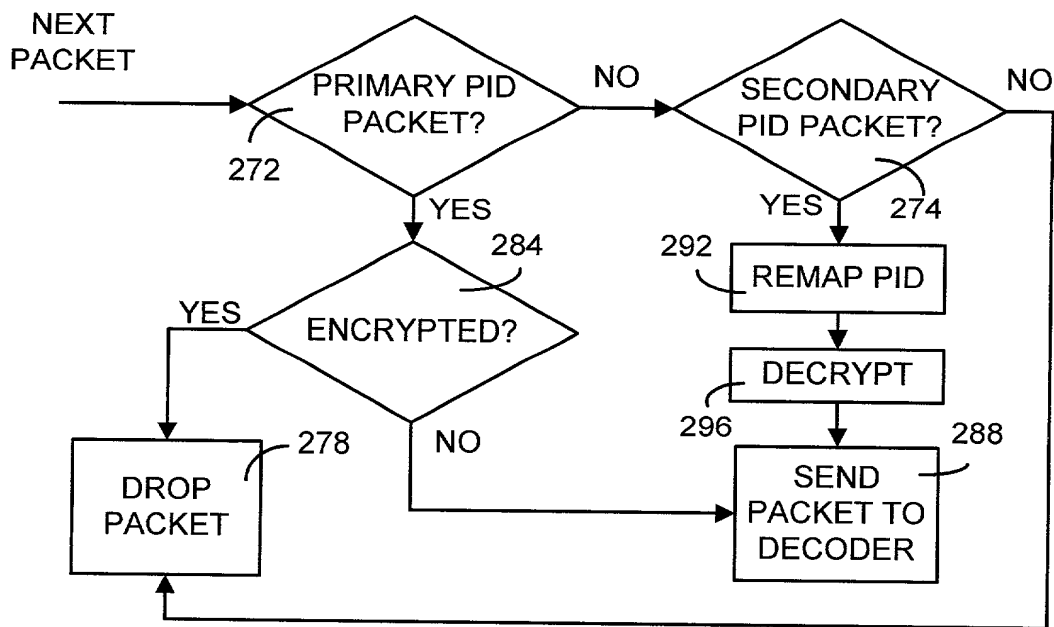


FIG. 5



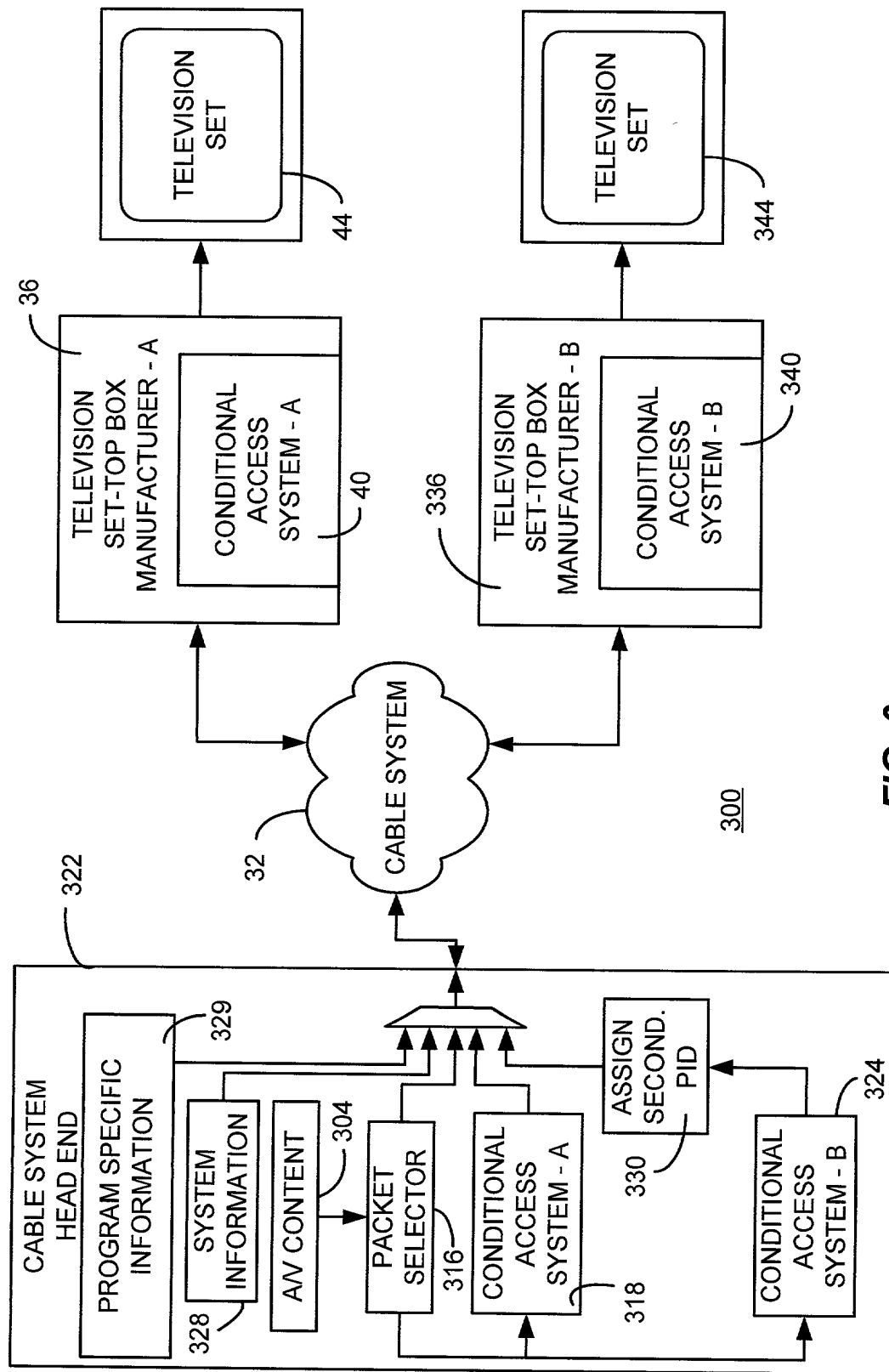


FIG. 6

FIG. 7

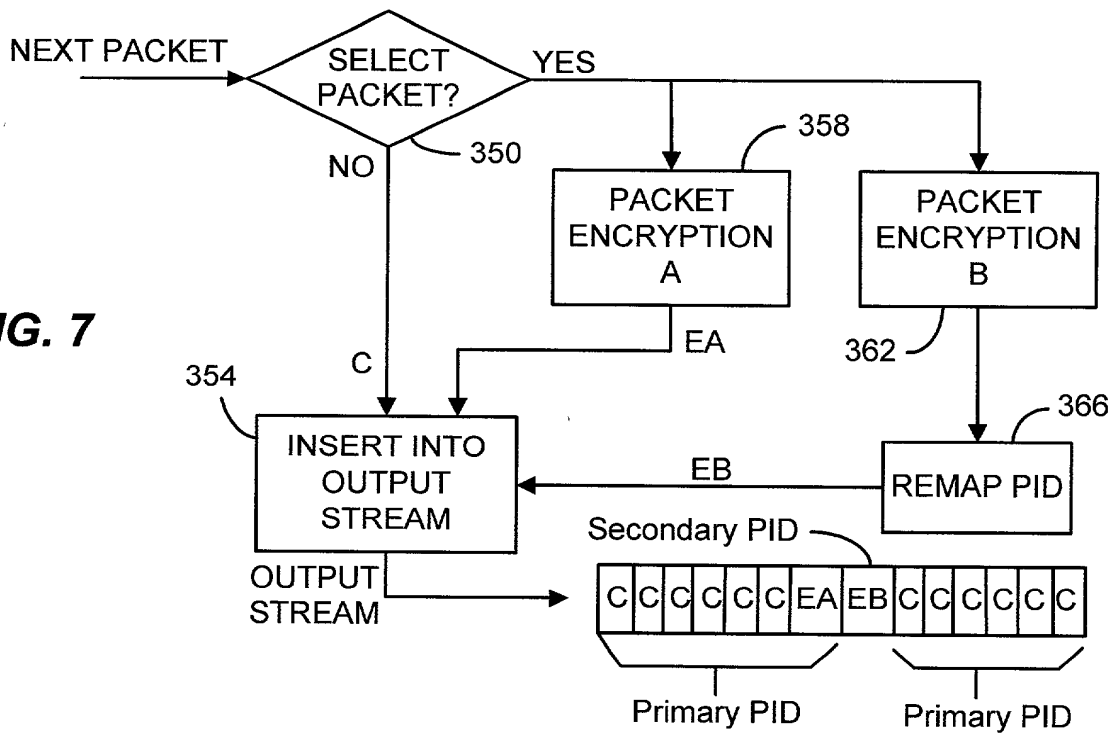
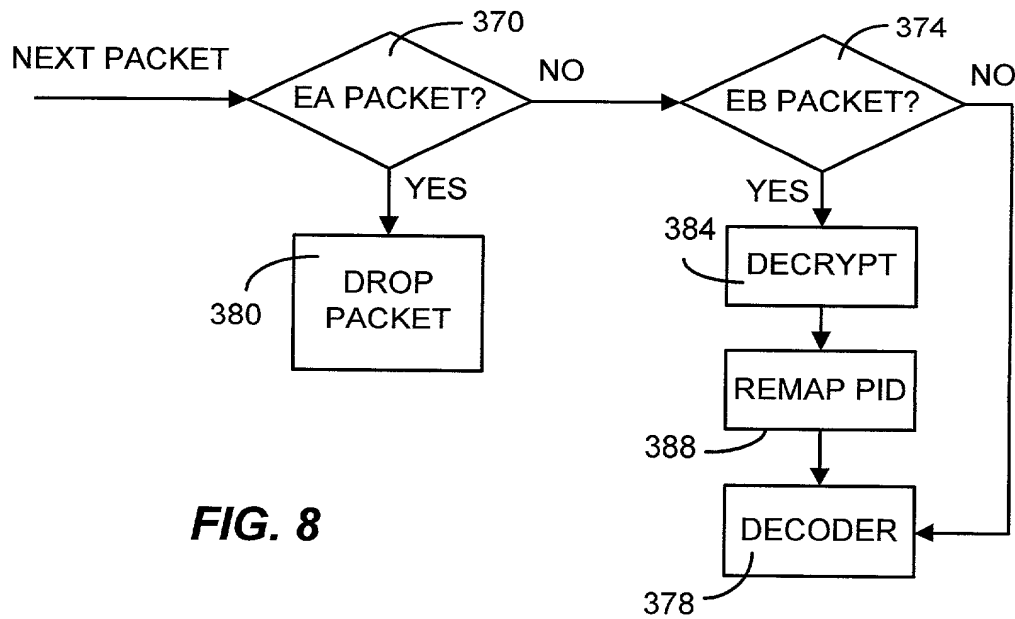


FIG. 8



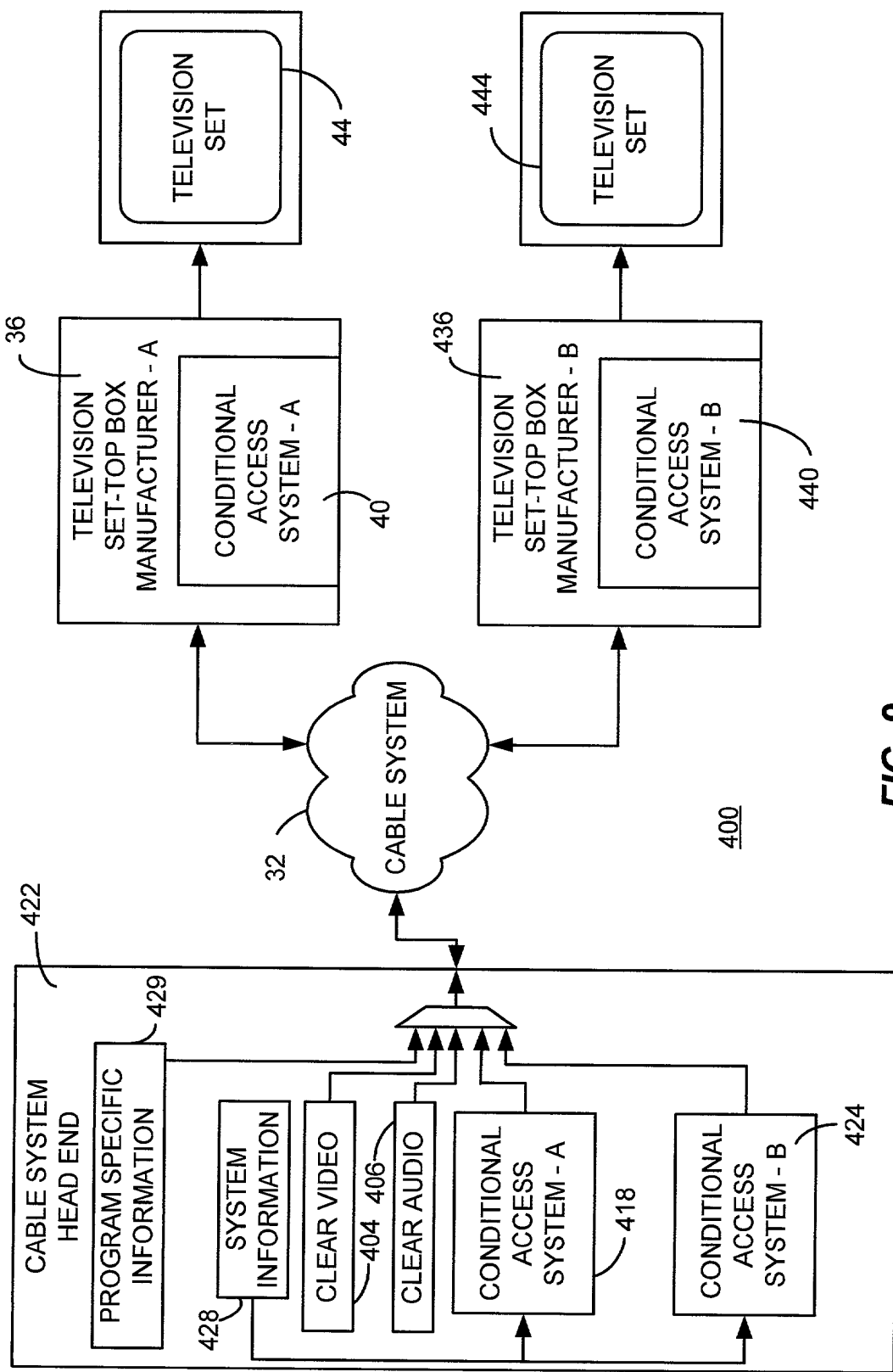


FIG. 9

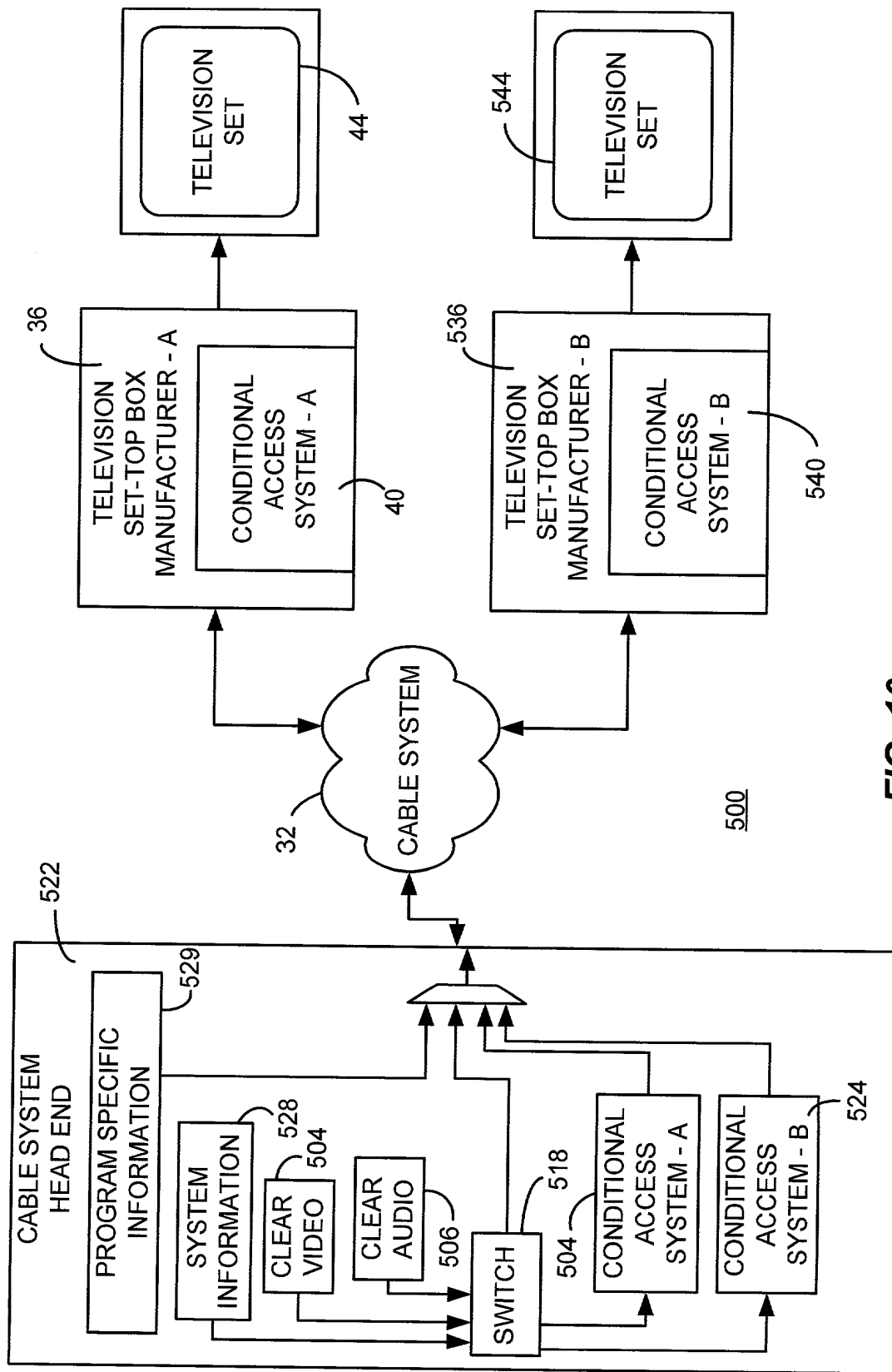


FIG. 10

FIG. 11 is a block diagram of a system for processing a hits feed. The system includes a receiver/descrambler/scrambler (604) that receives a hits feed (606) and outputs a signal to a legacy cable scrambler (612). The legacy cable scrambler (612) outputs a signal to a PID remap and scramble block (620). The PID remap and scramble block (620) outputs a signal to a QAM and RF block (628). The system also includes a packet selector/duplicator (610) that receives a signal from the receiver/descrambler/scrambler (604) and outputs a signal to a control system (614). The control system (614) outputs a signal to the PID remap and scramble block (620). The system also includes a control system (624) that outputs a signal to the PID remap and scramble block (620).

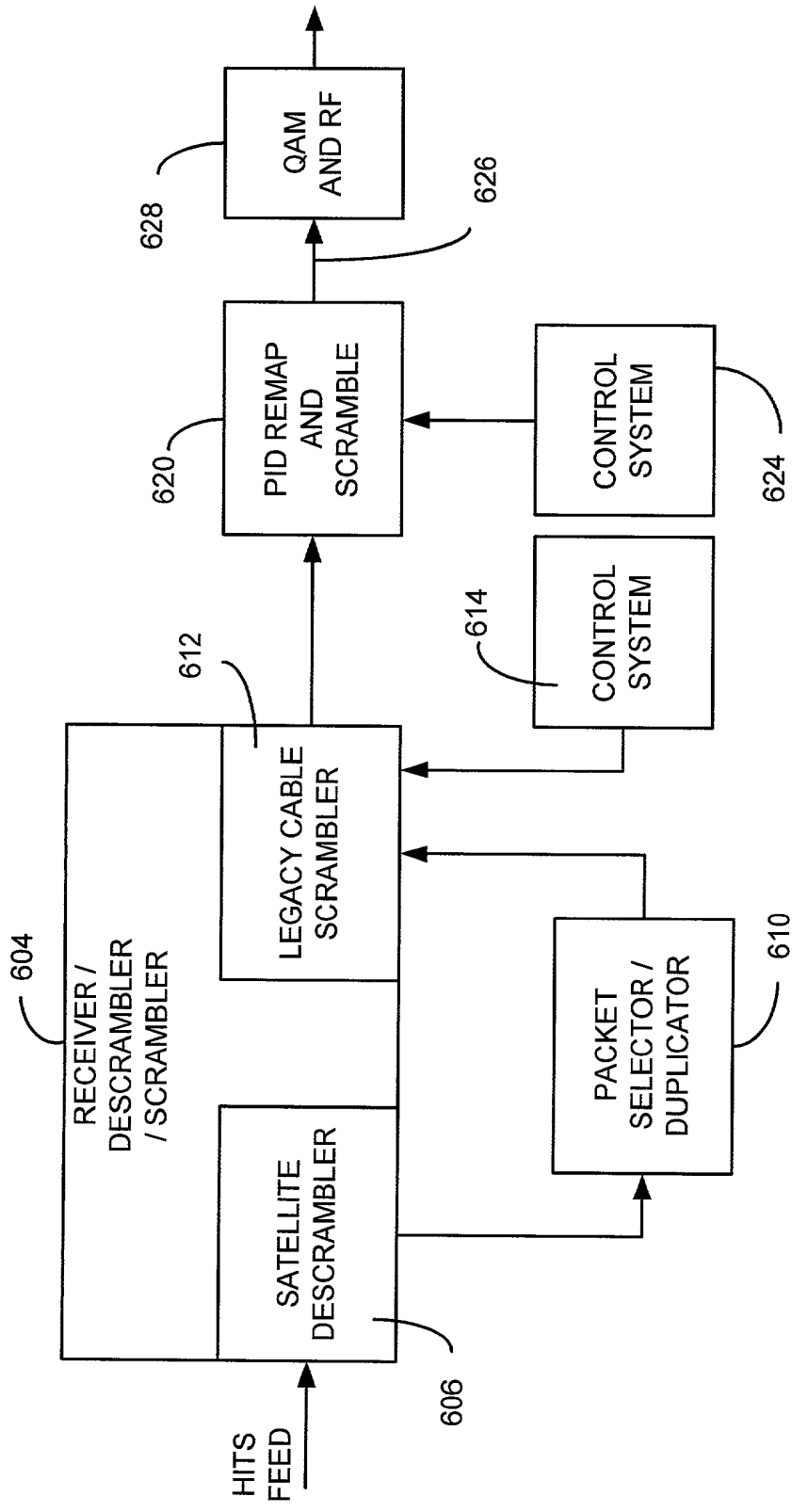


FIG. 11

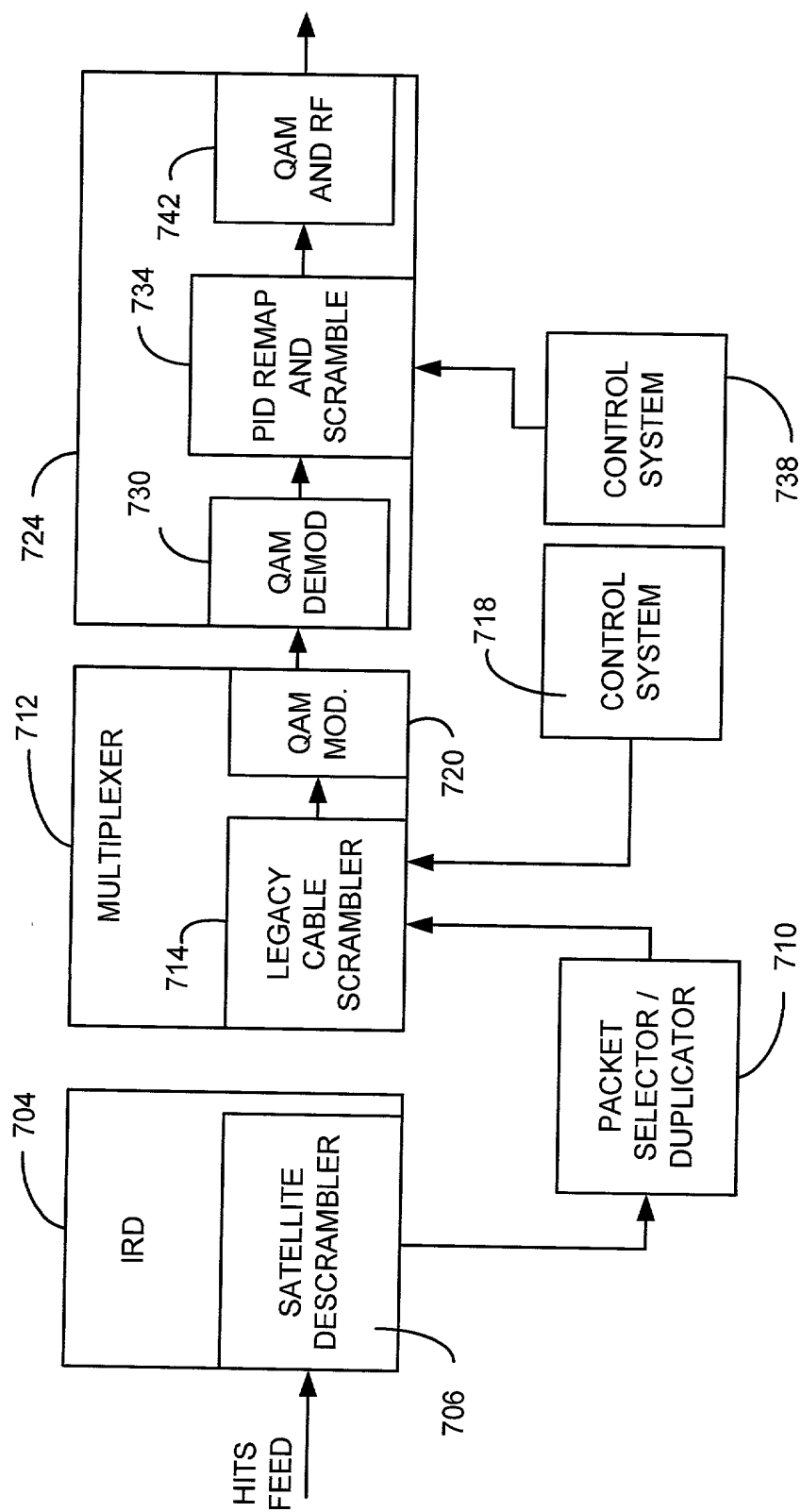


FIG. 12

FIG. 13

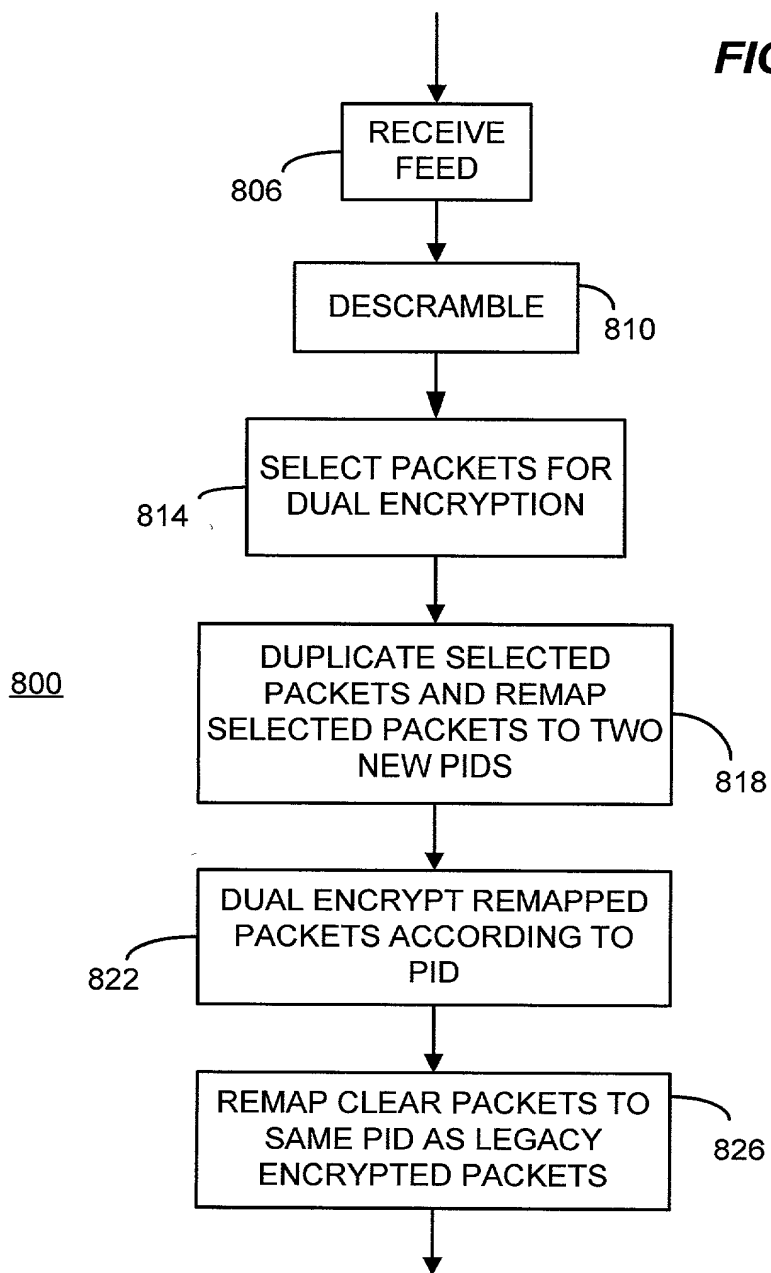


FIG. 14 is a block diagram of a system architecture for a set-top box or similar device. The diagram shows the following components and their interconnections:

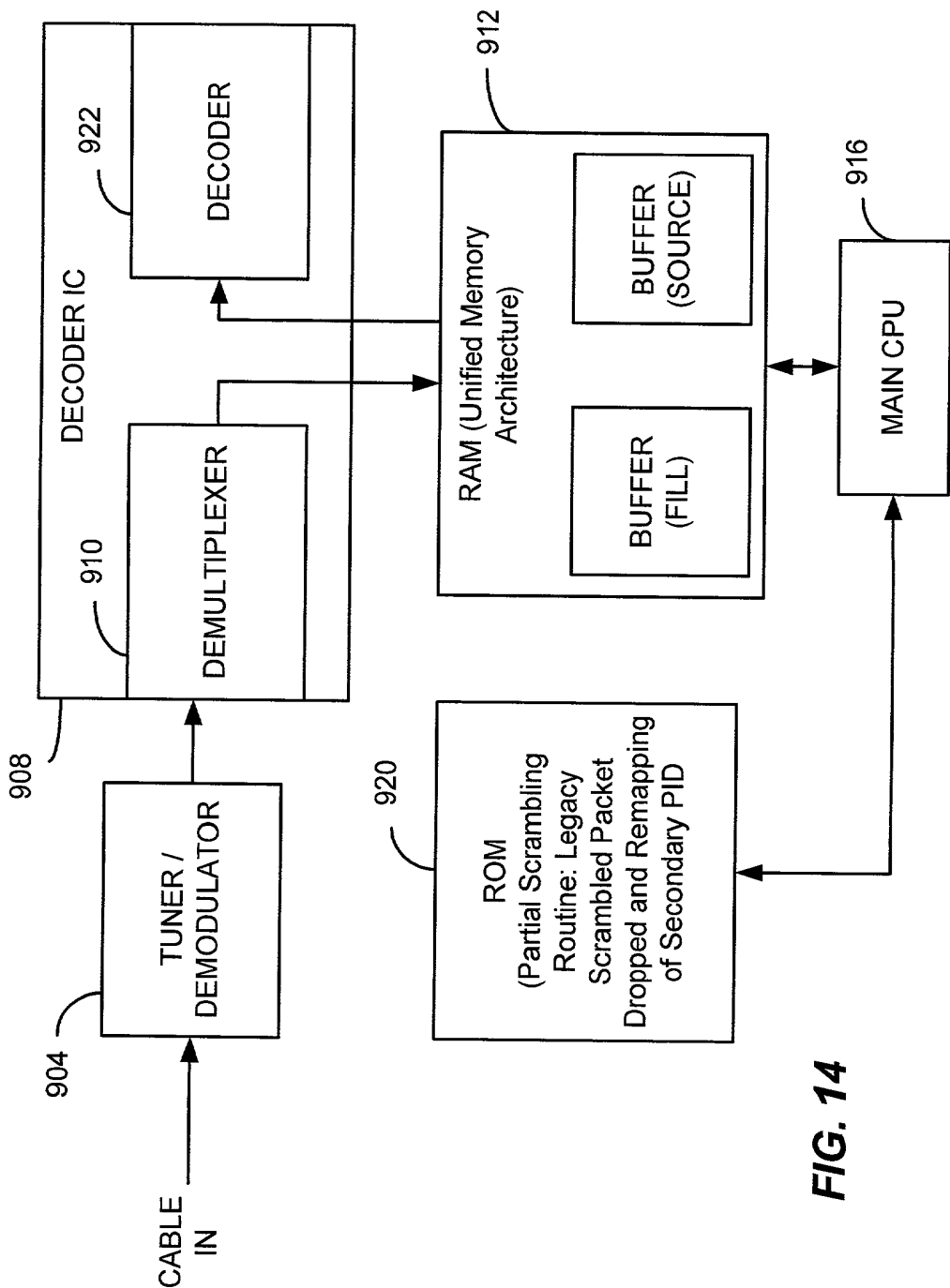


FIG. 14

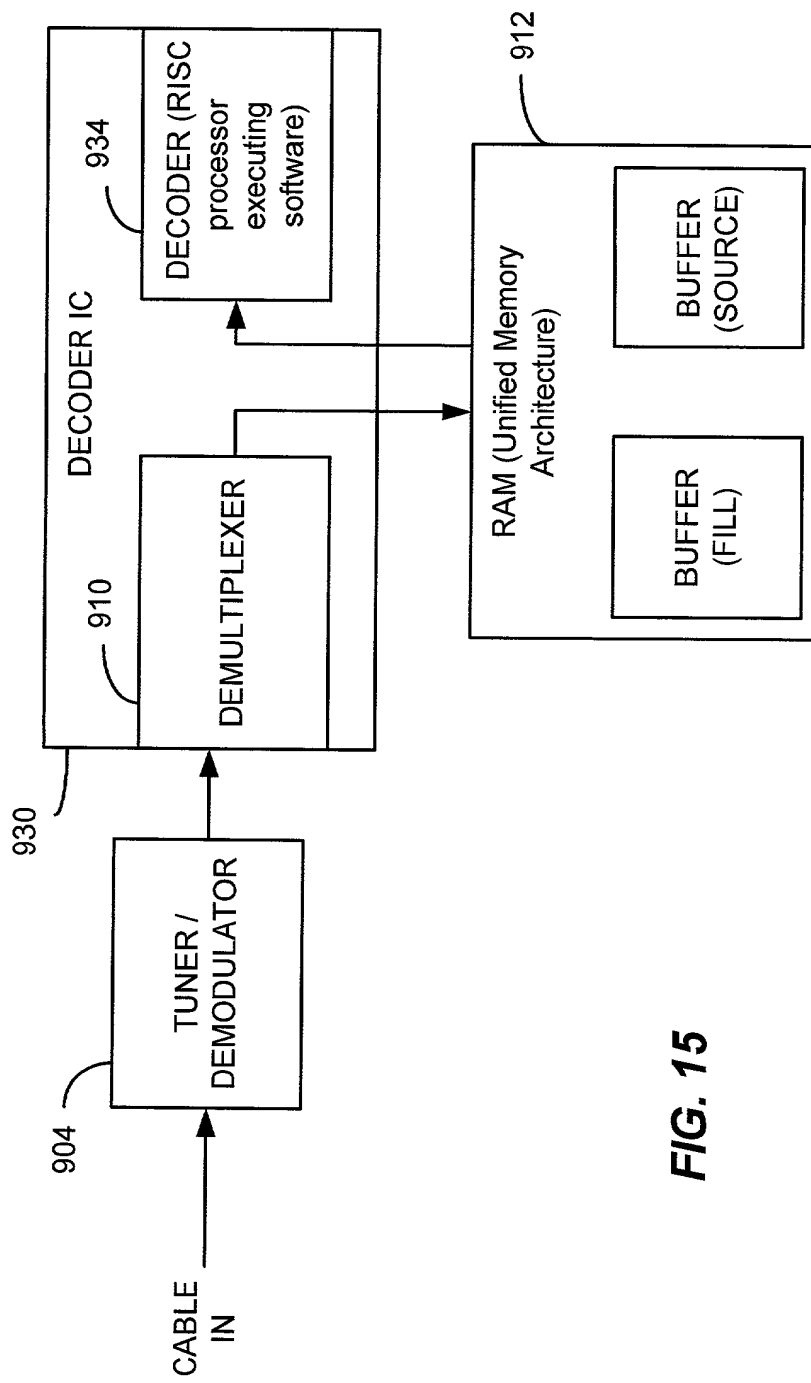
[illegible]

FIG. 15

FIG. 16 is a block diagram of a system architecture. The system includes a CABLE IN input, a TUNER / DEMODULATOR (904), a PLD (938), a DEMULTIPLEXER (940), a DECODER IC (908) containing a DECODER (922), and a RAM (Unified Memory Architecture) (912) with BUFFER (FILL) and BUFFER (SOURCE) components.

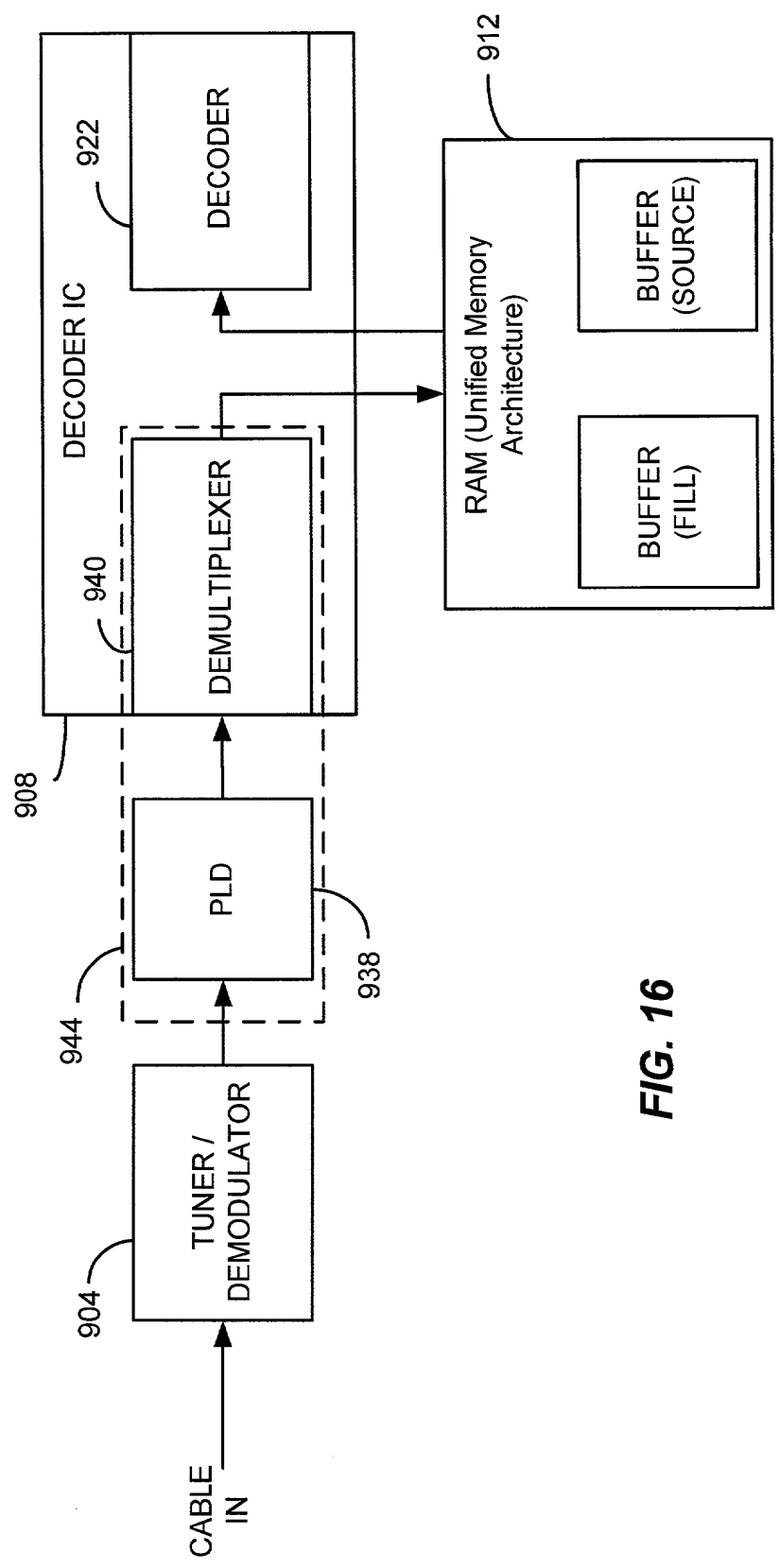
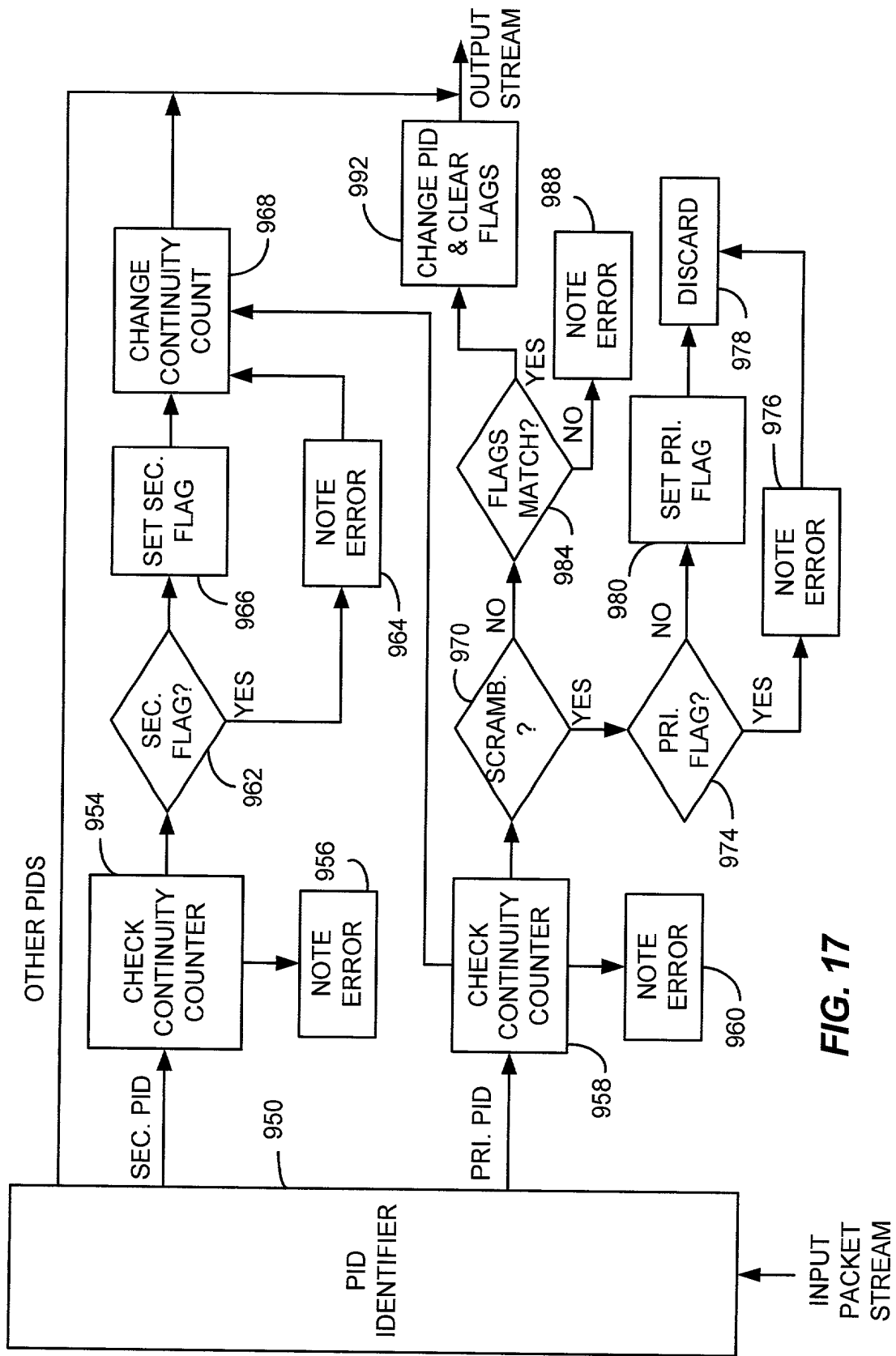


FIG. 16



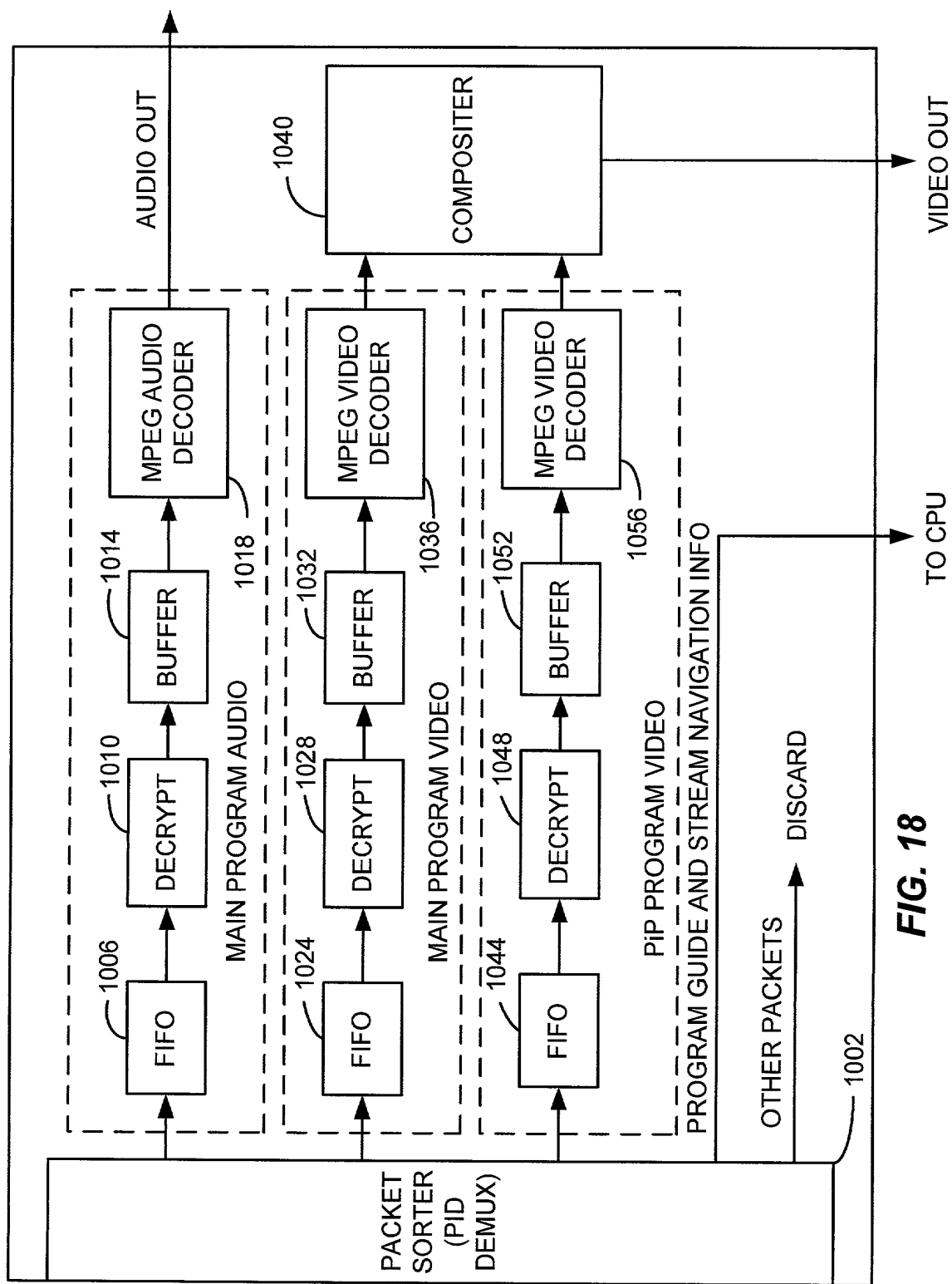


FIG. 18